On the Limits of the Capacitor-Voltage Active Damping for Grid-Connected Power Converters with *LCL* Filter

Javier Samanes and Eugenio Gubia
Electrical, Electronic and Communication Engineering, Institute of Smart Cities
Public University of Navarre
Pamplona, Spain
javier.samanes@unavarra.es

***Abstract*—Active damping strategies are widely extended to avoid stability issues at the *LCL* filter resonant poles in grid-connected voltage source converters. The capacitor voltage derivative active damping effectively damps the filter resonant poles without additional sensors, but it loses its effectiveness as the resonance frequency approaches the converter control Nyquist frequency, influenced by the existing delays in the control loop. To reduce this limitation, the delays can be reduced by performing a multisampled derivative, however, even though the stability limits might be extended, the oversampled approach might increase noise amplification problems. An appropriate filtering solution is required in the feedback path in order to reduce noise amplification and eliminate aliasing problems, without compromising the stability, as a result of a modification in the active damping feedback path. This work examines the limits of applicability of the capacitor voltage derivative strategy taking into account the filters used in the AD path, providing experimental results to validate the presented approach.**

***Index Terms*—Active damping, delay, capacitor-voltage-derivative, *LCL*-filter, stability.**

I. Introduction

The large number of renewable power plants has broadly extended the amount of grid-connected voltage source converters (VSC). To meet the grid operator requirements, VSC are frequently connected to the grid though a *LCL* output filter, reducing the presence of the switching harmonics in the grid current. However, with this filter, stability issues appear at the *LCL* resonance frequency, worsened by the high variability of the effective grid inductance at the point of common coupling (PCC). Passive and active damping (AD) methods can be implemented to solve the stability problems, where the latest are the preferred solution, as they avoid an increase in the converter power losses and in the filter complexity.

This work has been supported by the Spanish State Research Agency (AEI) and FEDER-UE under grant DPI2016-80641-R, and partially funded by the Public University of Navarre through a doctoral scholarship.

Active damping strategies have been widely developed in the literature, being the capacitor-current proportional feedback one of the most extended one [1]–[4]. This approach requires current sensors in the capacitor branches, which are not normally used. This current can be estimated from the capacitor voltage by derivation [5]–[7], as this voltage is normally measured to synchronize the VSC with the grid. The capacitor voltage derivative active damping (CVDAD) becomes less effective when the *LCL* resonance frequency approaches the converter current control Nyquist frequency, because the derivative action is distorted close to this limit [6]. Moreover, the effects of the delays introduced by the control loop and filters can produce instability. To further extend the limits of applicability of the CVDAD a faster derivative based on a multisampled approach can be used [8]. However, with a multisampled derivative, the high frequency noise and the switching harmonics are amplified, even more than with the conventional derivative.

This work explores the stability limits of the CVDAD for a robust operation against variations in the grid inductance. The influence of the filtering solution in the stability of the AD approach is analyzed, obtaining an analytical expression to evaluate the influence of the filters on the phase of the AD action, for both the multisampled and the conventional derivative, a critical aspect of the strategy. This expression requires reduced information on the power converter and the control loop. The AD filtering solution not only influences the stability of the power converter, it also affects the grid current quality, as aliasing might be an issue if the switching harmonics are not properly attenuated. The experimental results obtained for a 500 kW experimental setup validate the results obtained.

II. System Modeling and Control

A VSC connected to the grid is shown in Fig. 1. The *LCL* filter is formed by the converter inductance, L_c, the transformer leakage inductance, L_{transf} and the filter capacitor C_f. The grid effective inductance, L_g, depends on the impedance at the connection point [9]. The converter side current and the

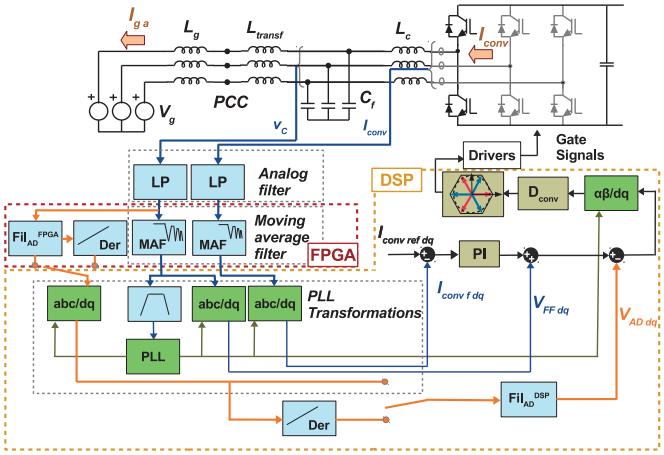

Fig. 1. Grid-connected power converter and control structure in the SRF.

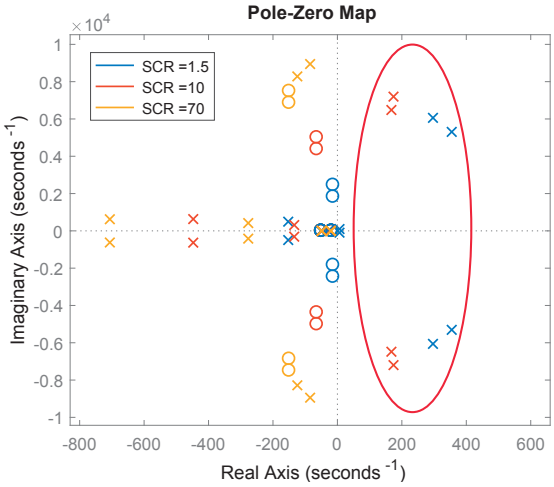

Fig. 2. Zero pole map of the system for three SCR = 1.5, 10 and 70.

capacitor voltage are measured and filtered by a first order low pass analog filter (LP(s)) and a digital moving average filter (MAF(s)) programmed in a field-programmable array (FPGA), which runs at a faster speed than the DSP. With this multisampled filter, the FPGA is able to eliminate the switching harmonic family and its multiples. The DSP performs asymmetrical sampling. The converter current control is performed in the synchronous reference frame (SRF) by means of a proportional integral controller (PI), used to achieve zero tracking error once that the fundamental component has been transformed to a DC component in *dq*. The PLL provides the angle for the Park transformation to the SRF. The voltage feedforward is used to reduce the variability of the plant, increasing the rejection to grid disturbances and, as a consequence, reducing high inrush currents. The delays introduced by the power converter, computation and zero order hold (ZOH), represented by $D_{conv}(s)$ in Fig. 1, are approximated by the expression derived in [10].

The system stability is studied in the SRF, so the the filters, LP(s) and MAF(s), as well as $D_{conv}(s)$ must be transformed to such frame. All the elements are transformed to the SRF using the transformation presented in [11]. Once that all the elements are expressed in the SRF, the closed loop poles and zeros are represented in Fig. 2, neglecting the AD feedback path represented in orange in Fig. 1. The stability is analyzed for three different short-circuit ratios, SCR, at the PCC; 1.5, 10 and 70. In this plot it can be seen that for weak grids, with SCR of 1.5 and 10, four unstable closed loop poles appear for each SCR. The instability at the *LCL* resonance frequency reveals that an AD strategy is required for the stable operation of the power converter in weak grids.

III. Implementation of the Capacitor Voltage Derivative Active Damping

In Fig. 1 the AD path is shown in orange. The derivative of the capacitor voltage, after being filtered by LP(s), is performed either in the DSP, executed at the same rate than the control loop, or in the FPGA, used to filter the measurements and running at a faster speed. The derivative action can be directly used to damp the resonance frequency, or digitally filtered in the FPGA with the filter Fil_{AD}^{FPGA} or in the DSP with Fil_{AD}^{DSP}.

The CVDAD strategy, as well as the capacitor current feedback AD, are equivalent to the implementation of a virtual resistance in parallel with the filter capacitor. Nevertheless, it has been reported in the literature that the influence of the delays in the control loop AD path transforms the virtual resistance into a virtual impedance [3], denoted by $Z_{AD}(s)$. Those transfer functions responsible of the transformation of the virtual resistance into a virtual impedance are the ones influencing the AD feedback; in Fig. 1 are LP(s), $Fil_{AD}^{FPGA}(s)$, $Fil_{AD}^{DSP}(s)$ and $D_{conv}(s)$. Moreover, the phase lost by the derivative as it approaches the control Nyquist frequency, aggravates this situation, particularly for the conventional implementation in the DSP. The expression for the emulated virtual impedance with the CVDAD is given in Eq.1, where the deformation of the derivative close to the control Nyquist frequency is represented by the transfer function $Der_{def}(s)$ and k stands for the constant multiplying the AD action.

$$Z_{AD}(s) = \frac{k}{LP(s)Fil_{AD}^{FPGA}(s)Fil_{AD}^{DSP}(s)D_{conv}(s)Der_{def}(s)} \quad (1)$$

The virtual impedance $Z_{AD}(j\omega)$, obtained by substituting s by $j\omega$ in Eq. 1, has a real, or resistive, component and an imaginary, or reactive, component. Both components vary with frequency, but the variations in the resistive component are specially important. As the effective grid inductance, L_g, changes depending on the connection point, the *LCL* resonant poles also vary. If within the range of frequencies where the resonance frequency is located, a change in the emulated resistive component occurs, the system is unstable for some

grid inductances. The sign of the emulated resistance can be either positive or negative, as long as it remains constant for the whole possible range of resonance frequencies, as the sign of the AD feedback path can be modified if a negative virtual resistance is emulated. A change in the emulated virtual resistance occurs every time that the phase of Eq. 1 equals $\pi/2$, for this reason the characterization of its phase is an important step. The phase of $D_{conv}(s)$ can be represented by a pure delay of 1.5 sample times. The low pass analog filter is a first order filter with a pole p_{LP}, while $Fil_{AD}^{FPGA}(s)$ and $Fil_{AD}^{DSP}(s)$ have not been defined yet, but in general, they can be defined as a product of zeros and poles. In the case of $Fil_{AD}^{FPGA}(s)$ a number of $n_{p\ FPGA}$ poles, p_{FPGA}, and $n_{z\ FPGA}$ zeros, z_{FPGA}, and in the case of $Fil_{AD}^{DSP}(s)$ as a number of $n_{p\ DSP}$ poles, p_{DSP}, and $n_{z\ DSP}$ zeros, z_{DSP}. At last $Der_{def}(s)$ introduces a pure delay of l_{der} sample times, which is 0 if the multisampled derivative is used and 0.5 if the derivative is implemented in the DSP. This approximation is valid, as demonstrated by Fig. 3. In this figure it is shown that the multisampled derivative behaves as an ideal derivative up to the DSP control Nyquist frequency while the derivative in the DSP can be modeled by the ideal derivative multiplied by half a sample period pure delay. With these considerations the phase of Eq. 1 can be expressed by Eq. 2.

$$\begin{aligned}\varphi(\omega) =&\omega T_{sDSP}(1.5+l_{der}) + \sum_{i=1}^{n_{pDSP}} atan\left(\frac{\omega}{p_{DSP_i}}\right)\\ &- \sum_{i=1}^{n_{zDSP}} atan\left(\frac{\omega}{z_{DSP_i}}\right) + \sum_{i=1}^{n_{pFPGA}} atan\left(\frac{\omega}{p_{FPGA_i}}\right)\\ &- \sum_{i=1}^{n_{zFPGA}} atan\left(\frac{\omega}{z_{FPGA_i}}\right) + atan\left(\frac{\omega}{p_{an}}\right) \qquad (2)\end{aligned}$$

where T_{sDSP} is the DSP sampling time.

In the following section, the effects of the filters used in the AD feedback path on the system stability and the grid current harmonic content is evaluated.

IV. Effects of the AD Filter and the Implementation of the Derivative on the Stability and Grid Current

As demonstrated in Eq. 2, the filter used in the AD path modifies the phase of the emulated virtual impedance, influencing the stability of the CVDAD. For this reason, in this section, the effect of different filtering solutions is evaluated. Not only the stability is assessed, but also the grid current quality is studied. This is done by performing experimental tests in the test bench shown in Fig. 4, implementing the CVDAD with both the multisampled and the conventional derivative, and each filtering solution evaluated. The test bench is a 500 kW grid-connected power converter, connected to a grid with a SCR of 10.

Three different filtering solutions are evaluated for the CVDAD:

1) First order low pass analog filter.

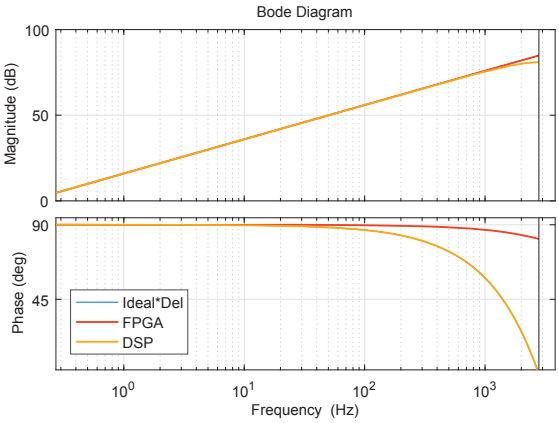

Fig. 3. Frequency response of the multisampled derivative, conventional derivative and the ideal derivative multiplied by a delay of half a DSP sample period.

2) First order low pass analog filter and moving average filter in the FPGA.
3) First order low pass analog filter and band pass filter in the DSP.

In the following, the effect of these filters in the resistive component of the emulated virtual impedance is evaluated. The limits evaluated in the following are absolute limits, meaning that if in this preliminary analysis the AD presents changes in the sign of the resistive component of the emulated virtual impedance, within the range of possible resonance frequencies, the system is unstable for some possible SCR. However, if no changes are produced in this range of possible resonance frequencies, it does not mean that the AD is able to stabilize the system, it means that it might be able to damp it with the appropriate AD constant, k_{AD}, adjusted. In Eq. 1 k is equal to L_c/k_{AD}.

The AD must be robust against variations in the grid inductance, as the SCR at the PCC varies from one location to

Fig. 4. Experimental set-up used for the validation of the CVDAD.

another. The variations in the SCR are limited between 1 and 300, the limits demanded in renewable energy industry. With this limits, an the parameters of the power converter used in the experimental setup, the resonance frequencies are bounded within 800 and 1520 Hz.

A. Low Pass Analog Filter

The first filtering solution used for the capacitor voltage in the AD path is a low pass first order analog filter, $LP(s)$, with a cut-off frequency of 3.5 kHz, shown in Fig. 5. In this way, $Fil_{AD}^{DSP}(s)$ and $Fil_{AD}^{FPGA}(s)$ in Eq. 1 are equal to 1. The phase in Eq. 2 is computed using this filtering option, representing the cosine of this phase in Fig. 6, or equivalently, the real part of $Z_{AD}(j\omega)$ for a unitary modulus. With this filtering option, the delay in the AD path is low, and the sign of the emulated virtual resistance has a reduced number of changes. However, with the possible range of resonance frequencies for the power converter under study, the multisampled approach presents a worse stability range than the conventional derivative, even though it can stabilize the system in a wider frequency range. As a result of a greater delay with the conventional derivative, the first change in the sign of the emulated virtual resistance occurs at lower frequencies, and within the range of possible *LCL* resonance frequencies it remains with the same sign. However, with the multisampled derivative, the first cross occurs at higher resonance frequencies, in the limit for the weakest grid considered. In this way, for the system under consideration, a lower delay implies reduced stability.

The SCR at the PCC of the test-bench is 10, meaning that the *LCL* resonance frequency is 950 Hz. With this measurement filter, and the multisampled derivative, there is not a k_{AD} that can effectively damp the resonant poles, and the system becomes unstable and is disconnected, as demonstrated in Fig. 7.

With the conventional derivative in the DSP, the AD is able to stabilize the resonant poles, but aliasing problems appear. In Fig.8 the grid current harmonic content is represented when the system is stabilized with the CVDAD and the conventional derivative. It can be seen that, at the *LCL* resonance frequency,

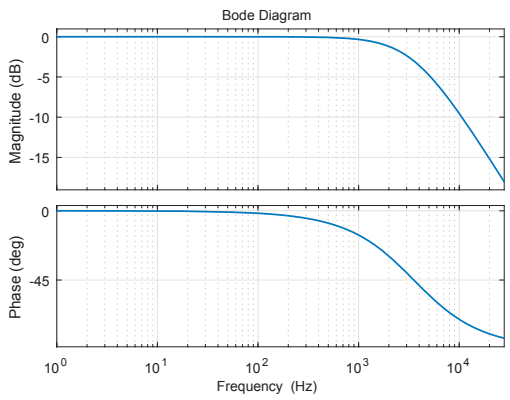

Fig. 5. Frequency response of the low pass analog filter.

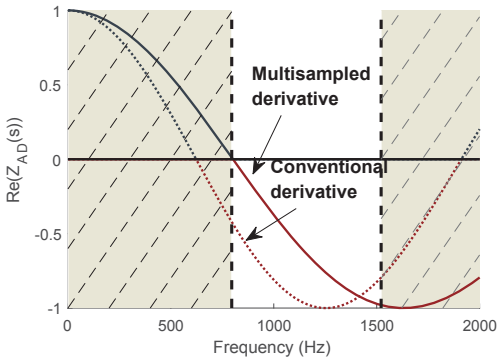

Fig. 6. Representation of the variation of the real part of the emulated virtual impedance as a function of frequency, for the multisampled and conventional derivative, using the LP filter.

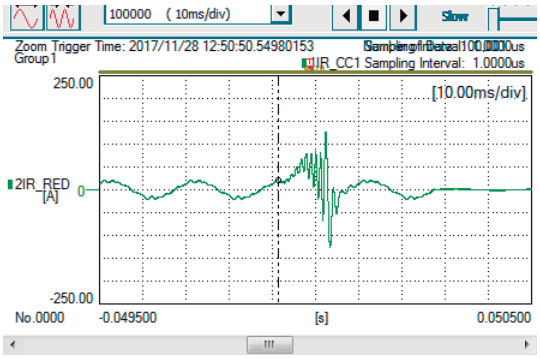

Fig. 7. Grid current with the LP filter and the multisampled CVDAD.

no significant harmonics appear, meaning that the filter resonance is properly damped. However, at low frequencies, two important harmonics appear at 250 Hz and 350 Hz.

The converter switching frequency is 2.8 kHz, sampling the capacitor voltage at twice the switching frequency, 5.6 kHz. The harmonics at higher frequencies than the control Nyquist frequency (equal to 2.8 kHz) are seen by the DSP as alias of the real frequency, at a frequency given by Eq. 3.

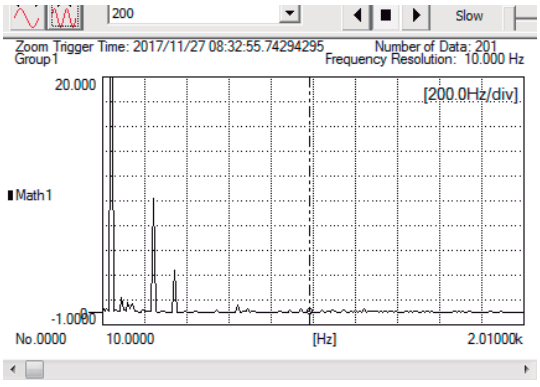

Fig. 8. Grid current harmonic content with the LP filter and the conventional CVDAD.

$$F_{alias} = |F - NF_{sDSP}| \tag{3}$$

Where F_{alias} is the frequency seen by the DSP, F is the real frequency and F_{sDSP} is the DSP sampling frequency. The harmonics of the second switching harmonic family are seen by the DSP at 250 and 350 Hz, creating the AD path two important current harmonics at 250 and 350 Hz, as a result of a poor filtering of the capacitor line voltage. It must be reminded that the rest of the control measurements are filtered by a MAF in the FPGA in order to eliminate the switching harmonic content.

B. Low Pass Analog Filter and Moving Average Filter in the FPGA

To avoid aliasing a MAF filter is applied in the FPGA to the capacitor voltage measurement. In this way, it is filtered by both $LP(s)$ and the MAF, given by Eq. 4. The frequency response of the resulting filter is shown in Fig. 9.

$$Fil_{AD}^{FPGA}(z) = \frac{1 - z^{-n}}{n(1 - z^{-1})} \tag{4}$$

Where *n* is the ratio of the FPGA sampling frequency and the power converter switching frequency. No additional filters are applied in the DSP, so $Fil_{AD}^{DSP}(s)$ is equal to 1.

$Fil_{AD}^{FPGA}(z)$ can be expressed in the continuous domain, calculating again the phase for the new AD filter and both derivatives. The real part of the emulated virtual impedance is shown in Fig. 10. In this case, the multisampled derivative offers a robust damping, while with the conventional derivative, a change in the sign of the emulated resistance occurs, and the AD will tend do destabilize the system if it is connected to strong grids.

In this case, the multisampled approach is a better option to robustly damp the system, so it is the option tested in the experimental setup. Fig. 11 shows the grid current harmonic content, proving that the resonance frequency is properly damped, as no significant harmonics are found at the resonance

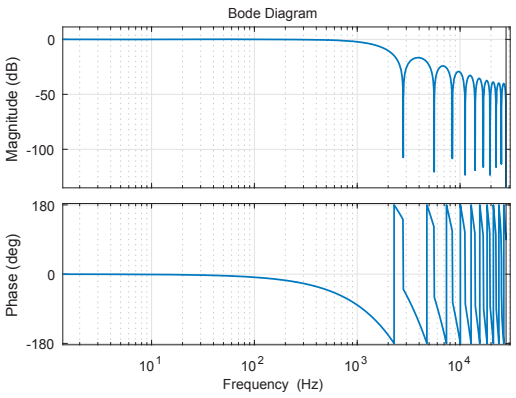

Fig. 9. Frequency response of the AD filter.

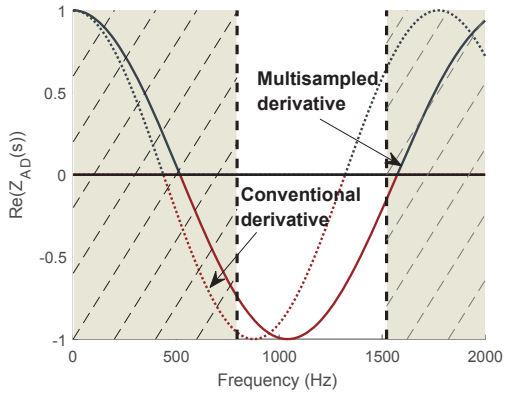

Fig. 10. Representation of the variation of the real part of the emulated virtual impedance as a function of frequency, for the multisampled and conventional derivative using the MAF and LP filters.

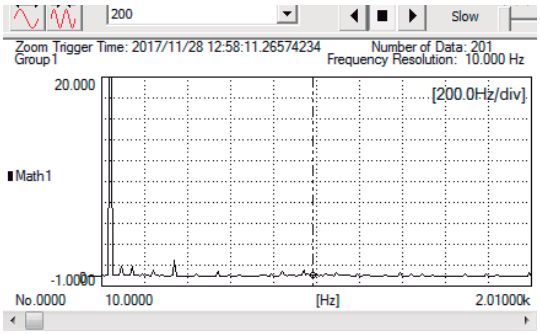

Fig. 11. Grid current harmonic content with the LP filter and MAF and the multisampled CVDAD.

frequency. The FPGA, where the MAF filter is implemented, runs ten times faster than the DSP, so the switching harmonics are properly attenuated and the low frequency alias, seen by the DSP, are almost negligible. In this way, the AD does not contain voltage harmonics at 250 Hz and 350 Hz, created when the capacitor voltage is sampled, and does not introduce low frequency harmonics in the grid current.

C. Low Pass Analog Filter and Band Pass Filter in the DSP

The MAF filter is able to eliminate aliasing problems, but it increases the delay in the AD path, compromising the stability of the CVDAD with the classical implementation of the derivative. For this reason, in order to reduce the delay introduced by the filter while still rejecting the low frequency alias, a band pass filter is implemented in the DSP, with $Fil_{AD}^{FPGA}(s)$ equal to 1. The resulting filter is the product of *LP(s)* and the band pass filter, obtaining the frequency response in Fig. 12 with the continuous equivalent transfer function of the band-pass filter.

The band pass filter is designed as a second order filter, fixing the low stop-band in order to introduce an attenuation of 9 dB at 300 Hz, and the high stop band set at the highest resonance frequency, 1500 Hz in this case.

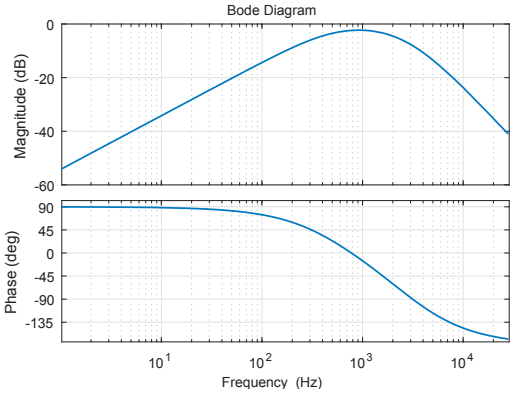

Fig. 12. Frequency response of the AD filter.

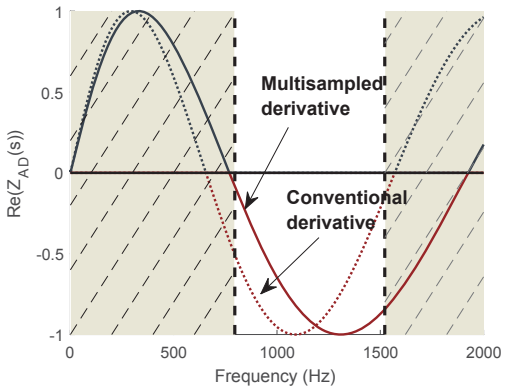

Fig. 13. Representation of the variation of the real part of the emulated virtual impedance as a function of frequency, for the multisampled and conventional derivative using the band-pass and LP filters.

With this filtering option, the conventional CVDAD presents greater stability margins for weak grids, while in strong grids it is close to a change in the sign, as shown in Fig. 13. With the multisampled CVDAD the system will be able to perfectly work in strong grid conditions, while it faces stability issues

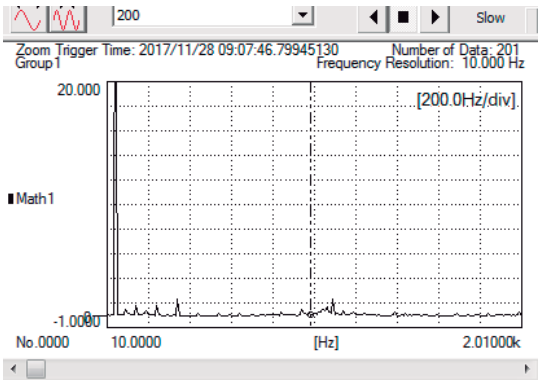

Fig. 14. Grid current harmonic content with the LP and band-pass filters and the conventional CVDAD.

in weak grids for the system under study.

If the grid current harmonic content is analyzed for the conventional derivative implementation, it can be seen in Fig. 14 that the resonant poles are properly damped, and aliasing problems are almost eliminated.

V. Conclusion

In this work an analysis of the robustness of the capacitor voltage derivative active damping strategy is performed for its conventional and multisampled implementation, depending on the filter used in the AD path. The *LCL* resonance frequency can suffer strong variations and the active damping must be robust to properly damp the system under all circumstances. As the effects of the delays may modify the sign of the emulated virtual impedance, causing stability problems, avoiding these variations is the first stability limit that the AD must face. The filter used in the AD path strongly influences this delay, and consequently the stability. But this filter is also important in order to avoid aliasing and noise amplification. Both, stability and aliasing aspects, are analyzed in this paper, providing experimental results to support the theoretical study. Depending on the system parameters and the range of possible resonance frequencies, a different filtering solution and implementation of the derivative has to be used, specifically studying the effects on the absolute stability limits and the grid current harmonic quality.

Acknowledgment

The authors gratefully acknowledge INGETEAM POWER TECHNOLOGY for its financial and ongoing support

References

[1] S. G. Parker, B. P. McGrath, and D. G. Holmes, "Regions of active damping control for lcl filters," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 424–432, 2014.

[2] J. Dannehl, F. W. Fuchs, S. Hansen, and P. B. Thøgersen, "Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters," *IEEE Transactions on Industry Applications*, vol. 46, no. 4, pp. 1509–1517, 2010.

[3] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of lcl-type grid-connected inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3414–3427, 2014.

[4] X. Wang, F. Blaabjerg, and P. C. Loh, "Virtual rc damping of lcl-filtered voltage source converters with extended selective harmonic compensation," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 4726–4737, 2015.

[5] M. Liserre, a. Dell'Aquila, and F. Blaabjerg, "Stability improvements of an LCL-filter based three-phase active rectifier," *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289)*, vol. 3, pp. 1195–1201, 2002.

[6] Z. Xin, P. C. Loh, X. Wang, F. Blaabjerg, and Y. Tang, "Highly Accurate Derivatives for LCL-Filtered Grid Converter With Capacitor Voltage Active Damping," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3612–3625, 2016.

[7] R. Peña-Alzola, M. Liserre, F. Blaabjerg, R. Sebastián, J. Dannehl, and F. W. Fuchs, "Systematic design of the lead-lag network method for active damping in lcl-filter based three phase converters," *IEEE Transactions on Industrial Informatics*, vol. 10, no. 1, pp. 43–52, 2014.

[8] J. Samanes and E. Gubia, "Multisampled-capacitor-voltage active damping for parallel interleaved grid connected voltage source converters with lcl filter," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*. IEEE, 2017, pp. P–1.

[9] J. L. Agorreta, M. Borrega, J. Lpez, and L. Marroyo, "Modeling and control of n -paralleled grid-connected inverters with lcl filter coupled due to grid impedance in pv plants," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 770–785, March 2011.

[10] J. Samanes and E. Gubia, "Sensorless active damping strategy for parallel interleaved voltage source power converters with lcl filter," in *Applied Power Electronics Conference and Exposition (APEC), 2017 IEEE*. IEEE, 2017, pp. 3632–3639.

[11] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 601–610, 2001.